Abstract

The present invention stacks chip scale-packaged integrated circuits (CSPs) into modules that conserve PWB or other board surface area. In a preferred embodiment in accordance with the invention, a form standard is disposed between the flex circuitry and the IC package over which a portion of the flex circuitry is laid. The form standard provides a physical form that allows many of the varying package sizes found in the broad family of CSP packages to be used to advantage while employing a standard connective flex circuitry design. In a preferred embodiment, the form standard will be bonded to the flex circuitry with metallurgical bonds devised from an intermetallic that improves module stability while lowering the module profile.